09-25-03 AF/2815 $ QC

Attorney's Docket No. 67,200-261 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ma et al
Serial No.: 09/ 821,521
Filed: March 29, 2001
For: Planar Spiral Inductor Structure with Patterned Microelectronic Structure Integral Thereto

Group Art Unit: 2815
Examiner: Matthew E. Warren

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Aug. 29, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$160.00
X	other than a small entity	$320.00

Appeal Brief fee due: $ 320.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))
I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 275 480 867 US in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313

Kathy Dixon

Dated: Sept. 23/03

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 390.00	$195.00
☐	three months	$ 930.00	$465.00
☐	four months	$1,470.00	$735.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 320.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 320.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 320.00
X Charge American Express Credit Card No. 3715 663193 71002 the sum of $ 320.00.
A duplicate copy of this transmittal is attached.

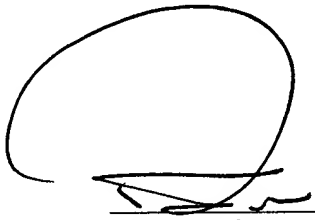
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

_X_ If any additional extension and/or fee is required, this is a request therefor to charge American Express Credit Card No. 3715 663193 71002

And/Or

_X_ If any additional fee for claims is required, please charge American Express Credit Card No. 3715 663193 71002



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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 21 September 2003

REF:

Applicant	:	Ma et al	Filing Date	:	29 March 2001
Serial No.	:	09/821,521	Att'y No.	:	67,200-261; TSMC 99-529/30
Art Unit	:	2815	Examiner	:	Matthew E. Warren
Title	:	Planar Spiral Inductor Structure With Patterned Microelectronic Structure Integral Thereto			

EXPRESS MAIL CERTIFICATE

Express Mail label Number EV 275 480 867 US
Date of Deposit Sept 23/03

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $320.00 (required filing fee) are being deposited with the United States Postal Service via Express Mail on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 29 May 2003 and made FINAL, applicant filed a notice of appeal on 29 August 2003. In accord with applicant's notice of appeal, please accept this appeal brief. No oral argument is requested.

09/29/2003 GBESHE1 00000042 09821521
01 FC:1402 320.00 OP

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 9 and 11-17 are pending in this application. Claims 9 and 11-17 are finally rejected under 35 U.S.C. § 103(a).

4. Status of the Amendments

A reply, filed 3 July 2003, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 28 July 2003, the Examiner indicated that applicant's response was considered but did not place applicant's application in condition for allowance since applicant's arguments were unpersuasive.

5. Summary of the Invention

The invention provides a method for fabricating a microelectronic inductor structure (in conjunction with optional microelectronic capacitor structure) within a

microelectronic fabrication, as well as the resulting microelectronic inductor structure (in conjunction with optional microelectronic capacitor structure). Within the invention, the microelectronic inductor structure (in conjunction with optional microelectronic capacitor structure) is fabricated with optimal performance while occupying minimal microelectronic substrate area. (paragraph 0025)

The invention realizes the foregoing objects by forming within the center of the microelectronic inductor structure a microelectronic structure (such as the optional microelectronic capacitor structure) comprising a series of electrically interconnected sub-patterns. (paragraph 0025)

The invention is claimed in: (1) a first level of scope directed towards the microelectronic structure formed in the center of the microelectronic inductor structure comprising a series of at least four electrically interconnected sub-patterns (independent claims 9 and 16 and claims dependent upon claim 9); and (2) a second level of scope directed towards a bond wire bonded upon the microelectronic structure (claims 15 and 17).

Independent claim 9 is read on the specification and drawings as follows:

9. (previously presented) A microelectronic fabrication comprising:

a substrate 10; (Fig. 1 and paragraph 0035) and

a spirally patterned conductor layer 12 formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure 14 formed within the center of the spirally patterned conductor layer 12, wherein the spirally patterned conductor layer 12 forms a planar spiral inductor, and wherein the microelectronic structure 14 formed within the

center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns. (Fig. 1 and paragraphs 0035 – 0036)

Independent claims 15-17 provide for: (1) the series of at least four electrically interconnected sub-patterns providing for attenuated eddy currents within the microelectronic structure; or (2) bonding a bond wire upon the microelectronic structure, where the bond wire has incorporated therein either a minimum of one or a plurality of loops.

6. Issues

I. Whether claims 9, 11-14 and 16 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson et al. (U.S. Patent No. 6,294,401; hereinafter "Jacobson") in view of Shiga (U.S. Patent No. 5,396,101).

II. Whether claims 15 and 17 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of DiCaprio et al. (U.S. Patent No. 6,452,278; hereinafter "DiCaprio").

7. Grouping of Claims

Claims 9, 11-14 and 16 are directed towards a first claimed embodiment of the invention.

Claims 15 and 17 are directed towards a second claimed embodiment of the invention.

The claims do not stand or fall together within their respective groups.

8. Arguments

I. The claims do not stand of fall together within their respective groups.

Applicant asserts that claim 17 contains subject matter (i.e., a plurality of loops within a bond wire) disclosed within neither Jacobson nor DiCaprio. Thus, in addition to applicant's responses below that are directed towards absence of suggestion or motivation to modify or combine Jacobson with DiCaprio such as to provide applicant's claimed invention, with respect to applicant's claim 17 applicant also asserts absence within Jacobson and DiCaprio of a teaching or suggestion of all limitations within applicant invention as disclosed and claimed within claim 17. Thus, applicant specifically requests independent consideration of each of applicant's claim 15 and claim 17.

II. Claims 9, 11-14 and 16 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of Shiga .

a. Jacobson Subject Matter

Jacobson (Fig. 4 and related text) teaches a planar spiral inductor structure comprising a patterned microelectronic structure terminating within the center of a spirally patterned conductor layer.

b. Shiga Subject Matter

Shiga (Fig. 2) teaches a planar spiral inductor structure having a patterned microelectronic structure formed within the center of the planar spiral inductor structure.

c. The Examiner's Assertions

The Examiner within the paragraph bridging pages 2-3 of the office action made FINAL acknowledges that Jacobson does not disclose a spirally patterned conductor layer having

formed within its center a microelectronic structure comprising a series of at least four electrically interconnected sub-patterns to attenuate eddy currents within the microelectronic structure (in accord with applicant's claim 9 and claim 16).

The Examiner at page 3, first partial paragraph, last sentence of the office action made FINAL predicates suggestion or motivation to modify or combine Jacobson with Shiga (to provide applicant's invention as disclosed and claimed within claim 9 and claim 16) upon Shiga's disclosure of attenuation of eddy currents within a microelectronic device such as to provide an increase in operating frequency of the microelectronic device.

d. Applicant's Response

In response, applicant notes that the Examiner has accurately cited Shiga's disclosure with respect to attenuation of eddy currents and increase in operating frequency within a microelectronic device. However, with respect to Jacobson, applicant notes that Jacobson's electronic identification tag (Fig. 4 and col. 7, lines 9-30) which comprises an inductor and a pair of interconnected capacitors is unlikely to experience eddy currents in its static state since there is no indication that Jacobson's electronic identification tag is powered in its static state. In addition applicant notes that Jacobson's electronic identification tag's response is a digital response provided at a resonant frequency and activated by a magnetic field from an external coil controlled by a separate logic circuit within Jacobson's electronic identification tag. Applicant is unable to locate within Jacobson any teaching or suggestion that eddy currents would actually occur incident to external magnetic field activation of Jacobson's electronic identification tag. Applicant is also unable to ascertain that additional patterning of Jacobson's pair of interconnected capacitors to effect eddy current attenuation would facilitate a desired result within Jacobson's electronic identification tag, such as an increased operating frequency, since

Jacobson's electronic identification tag operates at a resonant frequency which presumably need not necessarily be (and presumably is not) an increased operating frequency.

Thus, applicant asserts that Jacobson may not properly be modified or combined with Shiga to reject any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a) for reasons as suggested by the Examiner, since the reasons as suggested by the Examiner appear inapplicable to Jacobson's invention. The fact that references can be combined or modified is by itself insufficient suggestion or motivation for modification or combination of the references for providing a prima facie case of obviousness under 35 U.S.C. § 103. MPEP 2143.01.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 9, 11-14 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of Shiga be reversed.

II. Claims 15 and 17 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of DiCaprio.

a. Jacobson Subject Matter

As above.

b. DiCaprio Subject Matter

DiCaprio (cover figure) shows a microelectronic fabrication having formed therein a bond wire.

c. The Examiner's Assertions

The Examiner at page 4, lines 13-15 of the office action made FINAL predicates suggestion or motivation for modification or combination of Jacobson with DiCaprio (to provide applicant's claimed invention having a bond pad and a looped bond wire connected to the bond pad) upon DiCaprio's disclosure (col. 2, lines 48-50) of a desire to minimize a height of an electronics package.

d. Applicant's Response

In response, applicant asserts that there exists no suggestion or motivation for modification or combination of Jacobson with DiCaprio for reasons as suggested by the Examiner insofar as the reasons as suggested by the Examiner appear inapplicable to Jacobson's invention.

In that regard, applicant notes that Jacobson's electronic identification tag is activated by a magnetic field from an external coil and thus requires no apparent bond wire connection in a first instance. Thus, provision of a bond wire connection in the fashion as suggested by the Examiner would increase the height of Jacobson's electronics package, rather than minimizing the same, as suggested by the Examiner as rationale for suggestion or motivation for modification or combination of Jacobson with DiCaprio. In addition, applicant notes that applicant's multiply looped bond wire (as claimed within claim 17 and as is apparently not disclosed within either Jacobson or DiCaprio) would likely contribute to a further increase in height of an electronics package, rather than a decrease in height of the electronics package as suggested by the Examiner.

Thus, since the reasons as suggested by the Examiner for combining Jacobson with DiCaprio appear inapplicable to Jacobson invention, applicant asserts that Jacobson may not properly be combined with DiCaprio for purposes of rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 15 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of DiCaprio be reversed.

9. Summary

Applicant's invention as disclosed and claimed within claim 9, claim 15, claim 16 and claim 17 is directed towards a microelectronic fabrication, wherein the microelectronic fabrication comprises formed over a substrate a spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer forms a planar spiral inductor, and the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns (preferably at least four) to which may be bonded a bond wire having incorporated therein a minimum of one loop (and preferably a plurality of loops), such as to attenuate eddy currents within the microelectronic structure. The prior art of record employed in rejecting applicant's claims to applicant's invention may not properly be modified or combined for purposes of rejecting applicant's claims to applicant's invention, for reasons as suggested by the Examiner.

10. Conclusion

Applicant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims remaining within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,

Randy W. Tung (Reg. No. 31,311)

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APPENDIX

COMPLETE COPY OF THE CLAIMS

1. - 8. (canceled)

9. (previously presented) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns.

10. (canceled)

11. (original) The microelectronic fabrication of claim 9 wherein the microelectronic structure is selected from the group consisting of resistors, diodes, capacitors, bond pads and aggregates thereof.

12. (original) The microelectronic fabrication of claim 9 wherein the microelectronic structure comprises a capacitor electrically connected with a bond pad.

13. (original) The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed of a conductor material selected from the group consisting of non-magnetic

metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

14. (original) The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed in a geometric shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, an ellipse and a circle.

15. (previously presented) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns; and

a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a minimum of one loop.

16. (original) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the

spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns, such as to attenuate eddy currents within the microelectronic structure.

17. (previously presented) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns; and

a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a plurality of loops.